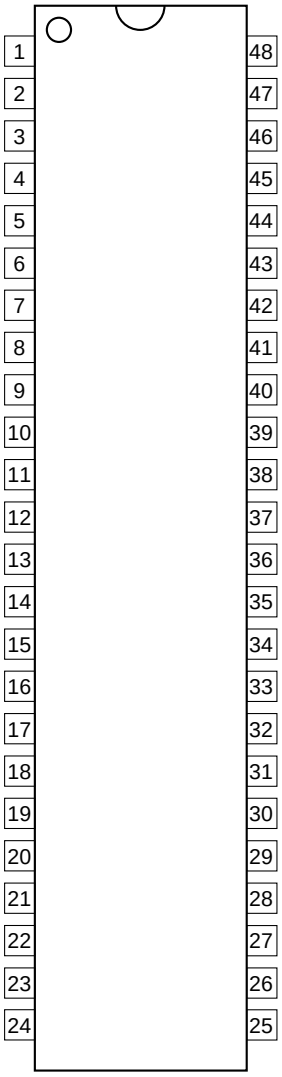
IEEE 1284 TRANSCEIVER

—TOP VIEW—



INPUTS

A9 - A13 : INPUTS
C14 - C17 : INPUTS
DIR : DIRECTION CONTROL
HD : HIGH DRIVE ENABLE
HLH_{IN} : HOST LOGIC HIGH INPUT
PLH_{IN} : PERIPHERAL LOGIC HIGH INPUT

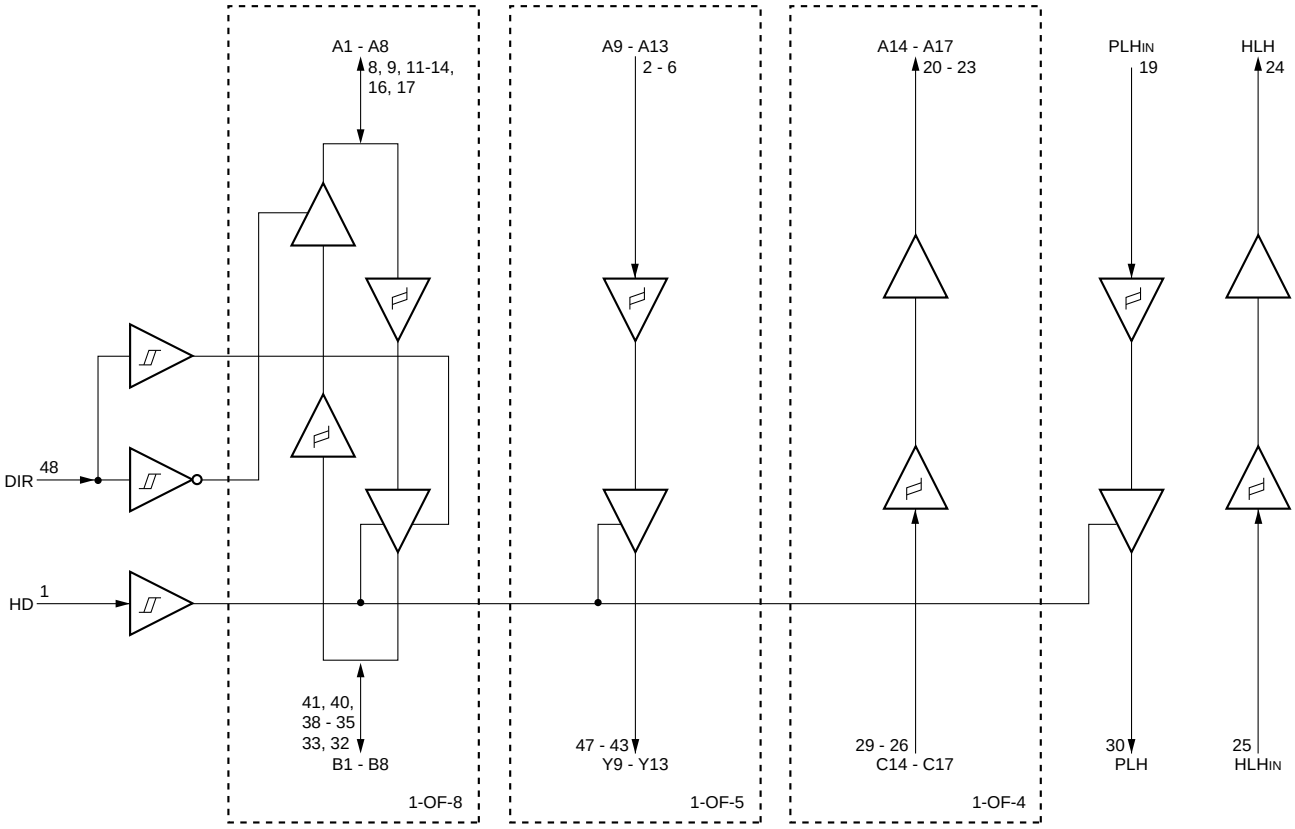
OUTPUTS

A14 - A17 : OUTPUTS
HLH : HOST LOGIC HIGH OUTPUT
PLH : PERIPHERAL LOGIC HIGH OUTPUT
Y9 - Y13 : OUTPUTS

INPUTS/OUTPUTS

A1 - A8 : INPUTS/OUTPUTS
B1 - B8 : INPUTS/OUTPUTS

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	HD	13	I/O	A5	25	I	HLH_{IN}	37	I/O	B4
2	I	A9	14	I/O	A6	26	I	C17	38	I/O	B3
3	I	A10	15	—	GND	27	I	C16	39	—	GND
4	I	A11	16	I/O	A7	28	I	C15	40	I/O	B2
5	I	A12	17	I/O	A8	29	I	C14	41	I/O	B1
6	I	A13	18	—	V_{CC}	30	O	PLH	42	—	V_{CC}
7	—	V_{CC}	19	I	PLH_{IN}	31	—	V_{CC}	43	O	Y13
8	I/O	A1	20	O	A14	32	I/O	B8	44	O	Y12
9	I/O	A2	21	O	A15	33	I/O	B7	45	O	Y11
10	—	GND	22	O	A16	34	—	GND	46	O	Y10
11	I/O	A3	23	O	A17	35	I/O	B6	47	O	Y9
12	I/O	A4	24	O	HLH	36	I/O	B5	48	I	DIR


A1 - A8
8, 9, 11-14,
16, 17
A9 - A13
2 - 6
A14 - A17
20 - 23
PLHIN
19
HLH
24
DIR
48
HD
1
41, 40,
38 - 35
33, 32
B1 - B8
47 - 43
Y9 - Y13
29 - 26
C14 - C17
30
PLH
25
HLHIN
1-OF-8
1-OF-5
1-OF-4